REMARKS

Claims 1-27 are all the claims pending in the present application and all claims stand rejected. Reconsideration and allowance of all pending claims are respectfully requested in view of the following remarks.

OBJECTIONS.

Drawings

Figure 2 is objected to as containing informalities. Namely, the Office Action alleges filter element 57 is shown as an amplifier as opposed to a filter. Respectfully, Applicant disagrees. Figure 2 does not represent a circuit level schematic but rather a block diagram of functional elements. A circuit level amplifier would be shown having 2 inputs. By way of contrast, a block diagram of a filter/amplifier is commonly designated in such block diagrams in the form of a triangle with a single input. In any respect, Applicant's specification makes clear that element 57 is a filter and the shape of the generic block designating this feature is irrelevant. Accordingly, Figure 2 is not believed to require correction again[1]. Reconsideration is respectfully requested.

CLAIM REJECTIONS.

35 U.S.C. § 112 (First Paragraph)

Claims 7-9 and 16 are rejected under the first paragraph of 35 U.S.C. § 112 as being non-enabling. Specifically, the Office Action alleges is not clear how the A/D converter + the ASK

[1] Applicant notes Fig. 2 was previously objected to in the Office Action dated April 8, 2004 and Applicant responded with appropriate corrections and replacement sheets.

modulator is reduced to a BPSK modulator or how the oscillator signal is implemented in the modulator. Applicant respectfully submits that the present rejection is improper since the Examiner has not met the burden of showing why Applicant's "presumptively accurate disclosure" would not enable one of ordinary skill in the art to make or use the invention recited in claims 7-9 and 16 without undue experimentation.

First, Applicant respectfully points out that neither a "1 bit" A/D converter nor a BPSK modulator is claimed by Applicant thus the rejection does not appear to have any actual bearing on the claims in this respect. Further, Applicant submits the skilled artisan readily recognizes how a modulator utilizes an oscillator signal to produce a modulated output. Since the Office Action has not provided any reasoning or evidence why the skilled artisan would not be able to make or use the invention claimed, *prima facie* non-enablement has not been established. See, e.g., *In re Wright*, 999 F.2d 1557 (Fed. Cir. 1993) (explaining criteria for rejection including why the patent office doubts the truth or accuracy of disclosure and providing evidence why the skilled artisan fails to teach how to make or use the claimed invention w/o undue experimentation).

For the foregoing reasons, Applicant respectfully requests reconsideration and withdrawal of this rejection.

35 U.S.C. § 102

Claims 1-3, 10-12, 14, 17-21, 23 and 25-27 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. 5,392,042 to Pellon. Applicant respectfully traverses this rejection for the following reasons.

The Office Action alleges Pellon discloses all of the limitations of these claims. Applicant respectfully disagrees. Pellon Figs. 1 and 2a discloses a conventional type of Sigma-Delta or Delta-Sigma analog to digital converter (DAC) which is an over-sampling system; that

is, it operates using a sample rate that is many timers higher than the Nyquist rate of its input signal. The A/D quantization inside the Sigma-Delta loop is very coarse (col. 2, ll. 3-5). The coarse quantization introduces a large amount of quantization noise inside the loop. The effect of the closed loop system is to attempt to drive the error signal at the output of the summer (202) to zero. The digital filter (108) following the Delta-Sigma loop (102) removes the out-of-band noise allowing the sample rate to be decimated down to something closer to the desired Nyquist rate.

In contrast to Applicant's claims, Pellon does not disclose or suggest an IF baseband down converter integrated with a Delta-Sigma loop. Accordingly, Pellon fails to teach or suggest at least the limitation in Applicant's claims including: *wherein the portable communicaton device is adapted to subtract the feedback signal from an IF signal.*

The Office Action points col. 11, ll. 16-19 of Pellon to show that IF sampling may be performed. However, Applicant respectfully submits that this does not meant that signal (x)t (Fig. 2A) is or could be an IF signal. As mentioned previously, in conventional Delta-sigma arrangements, the DAC 102 would be preceded by a down converter which may consists of a local oscillator and a mixer which would provide a I or Q signal to the DAC (i.e., the DAC would be duplicated on I and Q paths. Accordingly, the feedback loop 206 shown by Pellon is not subtracted from an IF signal as claimed by Applicant. Claims 19-27 have been amended to clarify this feature.

For at least the foregoing reasons, Applicant respectfully submits the rejection under 35 U.S.C. § 102(b) is improper and reconsideration and withdrawal of this rejection is respectfully requested.

35 U.S.C. § 103(a)

Claims 4-7, 9, 13, 15-16, 22 and 24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Pellon in view of the cited 1988 publication by Sklar and/or in further view of U.S. 6,577,674 to Ko. Applicant respectfully traverses these rejections for the following reasons.

The Office Action relies on Pellon to disclose the features of the rejected claims as applied above but admits Pellon does not specify the signal generator to be a modulator, an amplitude shift key modular, a multiplier adapted to multiply a local oscillator and a received signal.

The Office Action instead relies on Sklar and Ko to make up for these notable deficiencies alleging the combinations would be obvious for various reasons (e.g., that the Sklar modulator is analogous to the switching device described in Pellon; and/or to implement the multiplier and oscillator in Ko to further down convert). Applicant respectfully disagrees and submits that *prima facie* obviousness has not been established since (i) there is no proper motivation for combining the references as suggested; and (ii) even assuming it would be proper to combine the prior art as suggested, all the limitations present in Applicant's claims would not be taught or suggested.

(i) NO MOTIVATION TO COMBINE REFERENCES

Respectfully, it appears that the improper hindsight of Applicant's invention is the motivating factor for selectively picking and choosing elements from the cited references and combining them in piecemeal fashion. For example, Applicant is unaware of any reason, the skilled artisan would replace the switches disclosed in Pellon with a modulator. Further, the discreet insertion of oscillators and multipliers within the circuit of Pellon appears solely for the purposes of rendering the instant rejection as opposed to any logical rationale or suggestion to do so by Sklar or Ko. Applicant respectfully submits that the reason these elements are missing from Pellon entirely is that the down conversion of signals is performed (if performed at all) prior to reaching the Sigma-Delta ADC disclosed by Pellon. Accordingly, there is no need for

these elements in the Pellon system and thus weighs against the combination suggested in the Office Action.

(ii) ALL LIMIATONS ARE NOT DISCLOSED

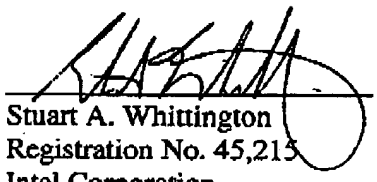
By virtue of Pellon not teaching or suggesting a device adapted to subtract the feedback signal from an IF signal discussed above, even when combining the prior art references as suggested in the Office Action, Applicant's recited limitations are not taught or suggested.

For all the foregoing reasons, Applicant submits the §103 rejections of record are improper and respectfully requests reconsideration and withdrawal of these rejections.

CONCLUSION.

In view of the above, reconsideration and allowance of this application is now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below. Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this case, and any required fee or deficiency thereof, except for the Issue Fee, is to be charged to **Deposit Account # 50-0221.**

Respectfully submitted,



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